Sem-II M. E ETC Microelectronics



RESULT REGISTER FOR M.E ELECTRONICS & TELECOMMUNICATION (MICROELECTRONICS) SEMESTER - II EXAMINATION HELD IN MAY 2017 Course: Revised Course - 2013

COLLEGE: GOA COLLEGE OF ENGINEERING Seat No: 3201 P R No: 201203659 Sex: F Name: NAIK ASHIKA RAMAKANT No Of Attempts: 1 No Of Grade **SGPA** Credits Obtained ASIC Design & FPGA p Theory 4 ΑB IΑ 2 AΑ Р Digital Signal Processors & Embedded Systems Theory 4 ΑВ Ρ 2 AΒ Design for Testability & E-Waste Management Theory ΑА IΑ AO Ρ Processor Architecture & Parallel Processing Theory AΑ ΙA ΑB Memory Design ВВ Theory Ρ IΑ AΑ Parallel Processing Lab IΑ ΑB Practical 2 ΑB FPGA & Embedded Systems Lab IΑ 2 BC Ρ Practical Ρ AΑ Total: 8.26 P PASSES 38 Seat No: 3202 PRNo: 201107721 Sex: F Name: PHADTE PRIYANKA DHARMA No Of Attempts: 1 No Of Grade **SGPA** Credits Obtained ASIC Design & FPGA ВС Theory 4 Þ IA 2 BB Ρ Digital Signal Processors & Embedded Systems Theory FF 4 2 BC Ρ IΑ Design for Testability & E-Waste Management Theory 4 BC P IΑ 2 AΒ Р Processor Architecture & Parallel Processing Theory FF ΙΑ 2 CC P Memory Design Theory ВС Р Α 2 BB Р Parallel Processing Lab Р IΑ 2 BC Ρ Practical 2 BC FPGA & Embedded Systems Lab IΑ 2 CC P Practical 2 AΒ Ρ Total: 4.95 F 38

FAILS



RESULT REGISTER FOR M.E ELECTRONICS & TELECOMMUNICATION (MICROELECTRONICS) SEMESTER - II EXAMINATION HELD IN MAY 2017 Course: Revised Course - 2013

COLLEGE: GOA COLLEGE OF ENGINEERING

t No: 3203 PR No: 20161166	6 Se	x:F	Nam	e: RA	SHINKAR PRAGATI GANAPATHI	
Of Attempts: 1		No Of Credits	Grac Obtai	_	SGPA	
ASIC Design & FPGA						
	Theory	4	BB	Ρ		
	IA	2	BB	Р		
Digital Signal Processors & Embedde	d Systems					
	Theory	4	BC	Ρ		
	IA	2	BB	Р		
Design for Testability & E-Waste Man	agement					
	Theory	4	CC	P		
	IA	2	BC	Р		
Processor Architecture & Parallel Pro-	cessing					
	Theory	4	FF	F		
	IA	2	CC	P		
Memory Design						
	Theory	4	AB	Р		
	IA	2	AB	Р		
Parallel Processing Lab				•		
	IΑ	2	BC	P	•	
	Practical	2	BC	Р	•	
FPGA & Embedded Systems Lab				*		
	IA	2	CC	Р		
	Practical	2	BB	Ρ		
	Total:	38	no en	anoimo area ano	5.74 F Result Reserve Sem I Not Passed	OLINIC POLITORING LO

Seat No: 3204	PRNo: 201107728	Sex	(: F	Nam	ie:	RODRIGUES FROILA VALENCY
No Of Attempts: 1			No Of Credits	Grad Obtai		SGPA
ASIC Design 8	& FPGA					
		Theory	4	BB	Ρ	
		IA	2	AA	Р	
Digital Signal	Processors & Embedded S	ystems				
		Theory	4	BC	Ρ	
		IA .	2	BB	Ρ	
Design for Tes	stability & E-Waste Manage	ment				
		Theory	4	AB	P	
		IA.	2	AO.	Р	
Processor Arc	hitecture & Parallel Process	sing				
		Theory	4	AB	Ρ	
		IA	2	AA	p	NIE
Memory Desig	ın					
		Theory	4	ВВ	Р	TALEIGAD
		IA .	2	AA	P	PLATEAU ,
Parallel Proce	ssing Lab					GOA JY
	•	IA	2 .	AA	Р	
		Practical	2	AA	P	
FPGA & Embe	edded Systems Lab		_	•	•	* 10 000
		IA	2	AA	Р	
		Practical	2	AO	P	
		Total:	38	e/A-ro*bo/intokritase dobnie wro.	conversion.	8.05 P PASSES

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Grade	Grade Points	Performance
AO	10	Outstanding
AA	9	Excellent
AB	8	Very Good
ВВ	7	Good
вс	6	Fair
CC	5	Satisfactory
FF	0	Fail

Read By :

Checked By: 📈

Date : 4/8/17

Vivek Salaskar Assistant Registrar-E(Proff.) Dr. Antifactifia Wagie Controller Of Examinations

Prof. Y. V. Reddy 418 Registrar

P: Passes; F: Fails; A/ABS: Absent; N/NAP: Non Appearance; X/NE: Not Eligible; +: Grades Carried Over; SGPA: Semester Grade Point Average; CGPA: Cummulative Grade Point Average